

## Signal Integrity and High Speed Methodology Training

Due to the great success of this training Sintecs is organizing this training class again in cooperation with Fast Edges Inc. and will be given by the Signal Integrity goeroe Mr. Rod Strange. The three day class will allow you to become familiar with signal integrity analysis at the board level. The lecture's modules address transmission lines and their effects on digital circuitry and printed circuit boards. The course will present detailed examples from real-world designs to demonstrate the necessity of understanding signal integrity issues and applying sound signal integrity principles to your PCB Design.

Date: **23, 24 and 25 April 2012**

Location: **Conference hotel Willibrordhaeghe, Deurne**

If you are interested please subscribe as soon as possible, seats are limited. You can use the registration form to register. You can also send an email to [info@sintecs.eu](mailto:info@sintecs.eu) or call us at +31 (0)74 2555713.

### **With this course you will gain a better understanding of the following:**

- Transmission lines and their effect on digital circuitry
- Printed circuit boards: drivers, receivers, Zo, Zdiff, stack up
- Quality board designs
- Termination, topology, timing, parasitics, etc
- Crosstalk: understanding and preventing
- Differential pair: termination, routing, timing, EMI
- Clock distribution, high speed busses, ground bounce
- Reference planes: ground, power, return currents, splits
- High speed layout: vias, connectors, capacitors, losses
- Testing issues: equipment, probes, test points
- Models: SPICE, IBIS, drivers, receivers, simulators and accuracy
- PCB simulations that detect signal integrity problems before fabrication

### **Audience**

- Digital Design Engineers
- ECAD Designers with some high speed experience
- Technicians with High Speed experience
- Those who would like to further their knowledge on Printed Circuit Board Signal Integrity issues.
- No advanced math is needed

### 3 day class syllabus

What is a transmission line?

What causes transmission lines?

What do they do to digital circuitry?

Avoiding transmission line problems

Transmission line effects

Undershoot & Overshoot – can destroy boards

Ring back, monotonicity, crosstalk, timing

Printed circuit boards

Stack up

Making controlled  $Z_0$

Controlled  $Z_0$  or controlled distance

Crosstalk problems with multiple vendors

Drivers, receivers,  $Z_0$

Strength & speed

$Z_0$  & drivers

Incident vs. reflected wave switching

Board interconnect delay

How is it different than system delay

Need to include interconnect delay in timing

How is it calculated?

Receiver input  $C$ , driver output  $R_s$ , PCB  $Z_0$ , etc

Reflected vs. incident wave switching

Termination

When is it necessary

Required to stop undershoot and overshoot

Placement and stub length

Parallel, series,  $Z_0$  matching, driver  $R_s$  matching

Diodes - dangerous

Topologies

When are topologies important

How do topologies affect signal integrity & timing?

Short & long Tee, star, daisy chain

Stub length

Package parasitics  
L's, C's, and R's  
How do they affect signal integrity & timing  
Capacitive loading on transmission lines

Differential pair  
Why are they important  
Noise and EMI  
Layout issues  
Zdiff, Zcomm, Zeven, & Zodd  
Controlling Zdiff  
Side to side vs broadside (over/under)  
Weak vs strong coupling  
Zdiff problems  
Skew affects on signal integrity & timing  
Better terminations  
How to make differential pair for > 3 GHz

Crosstalk  
What causes crosstalk?  
Routing densities  
Effects on timing & signal integrity  
Micro strip vs. strip line are different  
Same layer vs. dual strip line over/under  
Differential pair crosstalk  
Fixing crosstalk  
What needs to be done by layout engineers

Ground bounce - SSN  
What causes ground bounce?  
What does it do to driver & receiver voltage levels  
Problems with FPGAs and ASICs

PCB power integrity  
Planes  
Power & ground  
Spacing & location - loop inductance  
Bypass capacitors  
ESL  
Package & size  $\mu\text{F}$   
Spacing to load  
Location on PCB & empty spaces  
Mounting inductance, via placement, spacing, pads, etc

Reference planes  
Perforation  
Crossing splits  
Reference consistency in designs  
Vias, layer changes & references  
Controls routing & stack up

#### Connectors

- Controlled  $Z_0$ , geometry, pin outs
- Reference consistency
- Coupling
- How many grounds &  $V_{CC}$  - return currents

#### Vias

- $Z_0$  changes
- Reference changes
- Stub lengths
- Blind & buried vias
- Pads, antipads, hole diameter
- How to make a 10 GHz via

#### AC losses

- Skin effect & dielectric loss
- Micro strip vs. strip line
- Noise margins with differential pair
- Pre-emphasis & equalization

#### Layout issues

- Boards are becoming more difficult to layout
- What issues are important in today's fast boards for layout?
- PCBs are now part of the design

#### Testing issues

- Faster boards are harder to test
- How do you test them?
- What equipment do you need?
- How fast does the equipment need to be

#### S Parameters

- Frequency dependent descriptors
- Good for gigahertz designs
- S21 - Insertion loss or interconnect loss for SI
- Includes discontinuities, connectors, packages
- VNA - 2 & 4 port networks

#### IBIS models

- Drivers & receivers
- Simulators
- Accuracy
- Repairing & modifying

#### Quality board designs

- How to make quality boards
- What tools are needed?
- Signal integrity issues must be included