High-performance embedded systems

D&E event
Presenter: Hans Klos

AGENDA

- Introduction Sintecs
- Trends that make Electronic designs complex
- Electronic Design Challenges
- High-Speed Board Analysis
Introduction Sintecs

The Company Sintecs

- Started in 2000
- System design and services partner
- Core competences in electronic development, (embedded) software development and design analysis & verification
- System-On-Module supplier
Freescale Proven Partner

- Freescale proven partner since august 2014

- System on Module development
  - Freescale i.MX processor family
  - Freescale QorIQ processor family

- Custom electronic development
  - Integrate module in customer design

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Trends that make Electronic designs complex
**Trends**

- Shorter Rise & fall time
- Increasing Data Rate & Bandwidth
- Lower power supply voltage
- Higher currents
- Dense & larger pin count devices / smaller pitch

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**Rise & Fall times**

![Graph showing trend in rise and fall times](image)

- **1990**
- **2014**

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Increasing Data Rate

![Graph showing increasing data rate over time]

**DDRx supply overview**

![Bar chart comparing DDR, DDR2, DDR3, DDR4 supply voltage]

- **Vih – Vil**: 200 mV

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[Link to Sintecs website: www.sintecs.eu]
Dense & large pin count & smaller pitch devices

Electronic Design Challenges
Challenges

- PCB routing
- Packages
- Device loading
- Reference plane changes
- Number of power rails
- Multi Gigabit signaling

Rise & Fall times

Both are the same trace
Routing challenges

DDRx routing guidelines for a Xilinx Kintex 7

1. The maximum electrical delay between any DQ and its associated DQS/DQS# should be $\pm 5$ ps.
2. The maximum electrical delay between any address and control signals and the corresponding CK/CK# should be $\pm 25$ ps.
3. The maximum electrical delay of any DQS/DQS# should be less than that of CK/CK#.

DDRx timing simulation needed!

Packages

Example from the Xilinx Kintex 7 datasheet

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Device</th>
<th>Package</th>
<th>Value</th>
<th>Units</th>
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Notes:
1. These values are the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to derate the package.

168ps worst case package skew ~ 20 mm
Device loading

- DDR3 address line
  - 18 devices
  - Difference in loading: ~1.5 pF/device
  - 9 devices
  - Length compensation needed for matching timing

Reference plane change

- Return Current Across Reference Plane Change
  - What happens to Return Current in this Region?
  - Reference Planes
  - Displacement Current
  - Trace Current
Decoupling

IC: packaged die

Ceramic cap  Bulk cap  On-pkg cap  Die  Voltage Regulation Module

PCB

Number of Power Rails / Area fills

- Number of Power Rails / Area fills
- Small pitch BGA’s
- Planes are not low impedance any more
High-speed board analysis

Traditional electronic design flow
High-speed board analysis

Signal Integrity

Power Integrity

Thermal

DDRx timing analysis

DRC

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High-speed design flow

Component database:
Schematic symbols | Footprints | Simulation models (SI/PI/Thermal/Timing)

Design Idea
Design Technology
Specification
Detailed Design
PCB Floorplan
PCB Routing
Verification
Production
Final product

DFA
Thermal exploration
PI DC Drop
DFM

PI exploration
SI exploration
FPGA ID
DDRx Timing
SI Verification
PI AC decoupling

Design Constraints
PCB Technology | Electrical constraints | Physical constraints

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Design technology setup

- Explore which impedances are needed on the board
- How many signal and power planes are needed
  - What is smallest pitch of BGA's
  - How many power rails?

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</table>

Thermal analysis

- Early exploration of thermal behavior of your board
- Try to avoid to block the airflow with higher parts
- Don’t place e.g. critical parts above high power parts
- Start simulation before routing the board
Topology study

- Investigate
  - Component selection
  - Termination
  - Impedance
  - Routing topology
  - Length

- Develop constraints for driving PCB layout

Signal Integrity

- Signal over/undershoot
- Trace impedances
- Eye Pattern / Mask
- Crosstalk
- Monotonic signals
Power Integrity

**DC analysis**
- Voltage drop
- Current densities

**AC analysis**
- decoupling / Target impedance
- Plane noise

DDRx timing
**DDRx timing margins**

<table>
<thead>
<tr>
<th>DDRx</th>
<th>Data Valid Window</th>
<th>DRAM Margin</th>
<th>Package/Board Margin</th>
<th>Chip Margin</th>
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</table>

Only 93ps board/package margin ~10mm

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**Design Rule Checks**

- Trace crossing gaps
- IO coupling
- Reference plane change
- IC’s over split
- Traces near plane edge
- Decoupling placement
- Power/Ground width
- Long nets
- …..
Summary

✓ A good high-speed design starts with understanding different effects which can have impact on your design

✓ Try to develop first-time right
  ✓ When you plan 2 proto types, you will get 2 proto types

✓ Make use of high-speed board analysis tools

Thank you!

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