High-performance embedded systems

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AGENDA

- Introduction Sintecs
- Trends that make Electronic designs complex
- Electronic Design Challenges
- High-Speed Board Analysis
**Introduction Sintecs**

**The Company Sintecs**

- Started in 2000
- System design and services partner
- Core competences in electronic development, (embedded) software development and design analysis & verification
- System-On- Module supplier
Sintecs is a Freescale proven partner

- System on Module development
  - Freescale i.MX processor family
  - Freescale QorIQ processor family

- Custom electronic development
  - Integrate module in customer design

- High-speed board analysis

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Modules based on the Freescale i.MX series of application processors

- i.MX536 – Standalone or as module usable
- i.MX6 – SMARC module
Freescale QorIQ modules

- System On Modules based on the Freescale QorIQ T-series of processors (PowerPC).
  - T10xx modules
  - T2081 module

Trends that make Electronic designs complex
High-performance embedded systems

Trends

- Shorter Rise & fall time
- Increasing Data Rate & Bandwidth
- Lower power supply voltage
- Higher currents
- Dense & larger pin count devices / smaller pitch

Rise & Fall times

<table>
<thead>
<tr>
<th>Rise / fall times (ns)</th>
<th>1990</th>
<th>2014</th>
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</thead>
<tbody>
<tr>
<td>TTL / HCMOS</td>
<td>6</td>
<td>0.25</td>
</tr>
<tr>
<td>FCT</td>
<td>2</td>
<td>0.25</td>
</tr>
<tr>
<td>3.3V CMOS</td>
<td>2</td>
<td>0.25</td>
</tr>
<tr>
<td>65nm CMOS</td>
<td>1</td>
<td>0.25</td>
</tr>
<tr>
<td>45nm CMOS</td>
<td>1</td>
<td>0.25</td>
</tr>
<tr>
<td>32nm CMOS</td>
<td>1</td>
<td>0.25</td>
</tr>
<tr>
<td>10 Gbps SERDES</td>
<td>0.25</td>
<td>0.25</td>
</tr>
</tbody>
</table>
Increasing Data Rate

Max. data rate (Mbps)

Max. column cycle (MHz)

Year of Introduction

Increasing Bandwidth

Bandwidth (Gb/s)


USB 1.1 USB 2.0 Firewire eSATA USB 3.0 Compress USB 3.1 Thunderbolt 2

12Mb/s 0.48Gb/s 3 Gb/s 8.8Gb/s 25 Gb/s
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**DDRx supply overview**

![Bar chart showing supply voltages for DDR, DDR2, DDR3, and DDR4](chart)

- **VinL**: 200 mV
- **Vih - Vil**: 200 mV

**Electronic Design Challenges**
Challenges

- PCB routing
- Packages
- Device loading
- Reference plane changes
- Number of power rails
- Multi Gigabit signaling

Rise & Fall times

Both are the same trace
Routing challenges

DDR3 routing guidelines for a Xilinx Kintex 7

Match within a byte lane all the DQ, DM and DQS within 5ps → within less than 1 mm

- The maximum electrical delay between any DQ and its associated DQS/DQS# should be ±5 ps.
- The maximum electrical delay between any address and control signals and the corresponding CK/CK# should be ±25 ps.
- The maximum electrical delay of any DQS/DQS# should be less than that of CK/CK#.

DDRx timing simulation needed!

Packages

Example from the Xilinx Kintex 7 datasheet

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Package Skew</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>Device</td>
</tr>
<tr>
<td>Twocasey</td>
<td>Package Skew(2)</td>
</tr>
<tr>
<td></td>
<td></td>
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<td></td>
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</table>

Notes:
1. These values represent the worst-case skew between any two SelectIO resources in the package, shortest delay to longest delay from die to IO ball.
2. Package delay information is available for these device/package combinations. This information can be used to derate the package.

168ps worst case package skew ~ 20 mm
Device loading

**DDR3 address line**

- 18 devices
- ~1.5 pF / device
- Difference in loading

Length compensation needed for matching timing

**DDR3 clock line**

- 9 devices

Decoupling

IC: packaged die

- On-pkg cap
- Die

- Voltage Regulation Module

- Ceramic cap
- Bulk cap
- PCB
Number of Power Rails / Area fills

- Number of Power Rails / Area fills
- Small pitch BGA’s
- Planes are not low impedance any more

High-speed board analysis
High-performance embedded systems

Traditional electronic design flow

- Design Idea
- Detailed Design
- PCB Placement
- PCB Routing
- Production
- Proto 1
- Verification
- Design Update
- Production
- Proto 2
- Verification
- Design Update
- Production
- Final Product

High-speed board analysis

- Signal Integrity
- Thermal
- DDRx timing analysis
- Power Integrity
- DRC
High-speed design flow

Component database:
Schematic symbols | Footprints | Simulation models (SI/PI/Thermal/Timing)

Design idea
- Specification
- Detailed design
- PCB floorplan
- PCB routing
- Power distribution
- Design technology
- SI exploration
- PI exploration
- Thermal exploration
- Verification
- Production
- Final product

Design Constraints
- PCB Technology
- Electrical constraints
- Physical constraints

Design technology setup

- Explore which impedances are needed on the board
- How many signal and power planes are needed
  - What is smallest pitch of BGA’s
  - How many power rails?

<table>
<thead>
<tr>
<th>Layer</th>
<th>Stack-up</th>
<th>Width</th>
<th>Spacing</th>
<th>Min</th>
<th>Max</th>
<th>Min Width</th>
<th>Min Trace</th>
<th>Min Space</th>
<th>Min Trace</th>
<th>Min Space</th>
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</thead>
<tbody>
<tr>
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<td>0.055</td>
<td>0.050</td>
<td>0.035</td>
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<td>0.045</td>
<td>0.110</td>
<td>0.045</td>
<td>0.110</td>
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<tr>
<td>2</td>
<td>Cu/FR4/FR4/Cu</td>
<td>0.055</td>
<td>0.050</td>
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<td>0.130</td>
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<td>0.055</td>
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<tr>
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<td>0.050</td>
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<td>0.130</td>
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<tr>
<td>5</td>
<td>Cu/FR4/FR4/Cu</td>
<td>0.055</td>
<td>0.050</td>
<td>0.035</td>
<td>0.130</td>
<td>0.045</td>
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<tr>
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<tr>
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<tr>
<td>8</td>
<td>Cu/FR4/FR4/Cu</td>
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<tr>
<td>9</td>
<td>Cu/FR4/FR4/Cu</td>
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<td>10</td>
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Hans Klos – Sintecs BV, November 2014
**Thermal analysis**

- Early exploration of thermal behavior of your board
- Try to avoid to block the airflow with higher parts
- Don’t place e.g. critical parts above high power parts
- Start simulation before routing the board

**Signal Integrity**

- Signal over/undershoot
- Trace impedances
- Eye Pattern / Mask
- Crosstalk
- Monotonic signals
First, we only had 1 power and 1 ground pin
✓ A capacitor was placed across the IC to provide local current

Then we got 1 or 2 voltage rails
✓ 3.3V, 5V and each power rail gets its own plane

Current digital circuits
✓ More different power rails, 0.9V, 1.2V, 1.35V, 1.5V, 1.8V, etc.

Planes chopped up into several islands
✓ IC’s with >250 power and ground pins

✓ Power Integrity analyses needed

✓ DC analysis
✓ Voltage drop
✓ Current densities

✓ AC analysis
✓ Decoupling / Target impedance
✓ Plane noise
High-performance embedded systems

**DDRx timing**

Only 93ps board/package margin ~10mm

**DDRx timing margins**

<table>
<thead>
<tr>
<th>DDR</th>
<th>Data Valid Window</th>
<th>DRAM Margin</th>
<th>Package/Board Margin</th>
<th>Chip Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR1</td>
<td>2,500</td>
<td>900</td>
<td>800</td>
<td>800</td>
</tr>
<tr>
<td>DDR2</td>
<td>936</td>
<td>425</td>
<td>256</td>
<td>256</td>
</tr>
<tr>
<td>DDR3</td>
<td>469</td>
<td>188</td>
<td>140</td>
<td>140</td>
</tr>
<tr>
<td>DDR4</td>
<td>313</td>
<td>125</td>
<td>93</td>
<td>93</td>
</tr>
</tbody>
</table>

400 Mbps  → 3,200 Mbps
Design Rule Checks

Use Design Rules checker for e.g. following:

- Trace crossing gaps
- IO coupling
- Reference plane change
- IC’s over split
- Traces near plane edge
- Decoupling placement
- Power/Ground width
- Long nets
- …..
Summary

- A good high-speed design starts with understanding different effects which can have impact on your design
- Try to develop first-time right
  - When you plan 2 prototypes, you will get 2 prototypes
- Make use of high-speed board analysis tools

Thank you!

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